Pokhara University

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| Level: Bachelor | Semester: Fall | Year : 2015 |
| Programme: BE | | Full Marks: 100 |
| Course: Computer Organization and Architecture | | Pass Marks: 45 |
| Time : 3hrs. |

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| *Candidates are required to give their answers in their own words as far as practicable.* |
| *The figures in the margin indicate full marks.* |
| Attempt all the questions. |

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|  | 1. Describe the assembly process for assembly-language programs. How does it differ from the compilation process? 2. How a 16 X 2 memory subsystem can be constructed from two 8 x2 ROM chips with low-order interleaving? Explain. | 8  7 |
|  | 1. Design a very simple CPU that has 6-bit address register (AR), 6-bit program counter (PC), 8-bit data register (DR) and 2-bit instruction register (IR). The CPU must execute the following instructions:  |  |  |  | | --- | --- | --- | | Instruction | Instruction Code | Operation | | COM | 00XXXXXX | ACAC' | | AND | 01AAAAAA | ACACM[AAAAAA] | | JREL | 10AAAAAA | PCPC+AAAAAA | | SKIP | 11XXXXXX | PCPC+1 |  1. Explain the different sections of VHDL design code. Write VHDL code for D-Flip-flop. | 8  7 |
|  | 1. A computer system with an 8-bit address bus and an 8-bit data bus uses isolated I/O. It has 128 bytes ROM starting at address 00H constructed using 32×8 chips; 64 bytes of RAM starting at address 80H constructed using 64×4 chips. Show the design for this system. 2. Multiply (4)10 by (-2)10 by using Booth’s algorithm. | 8  7 |
|  | 1. What are the significance of cache memory? Write different types of mapping technique. 2. Differentiate between Segmentation and Paging? Describe the four most common replacement algorithms related to design issues of cache memory? | 7  8 |
|  | 1. How DMA controller can be incorporated in a computer system? 2. Explain major set of design principles related to RISC architecture. Calculate the window size and total number of registers. Given: No. of Global registers=10, No. of Local registers=10, No. of common registers=6, No. of windows=4. | 8  7 |
|  | 1. What is an interrupt? How is an interrupt serviced? Explain software actions in interrupt handling. 2. Define Mesh Topology. Describe different memory organization of multiprocessor system. | 8  7 |
|  | Write short notes on: (**Any two**)   1. MIMD Architecture. 2. Arithmetic pipelining. 3. Register Windows. | 2×5 |